

Notice of Allowability

Application No.

10/789,903

Applicant(s)

MCLEOD ET AL.

Examiner

Art Unit

Jean B Jeanglaude

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 02-27-04.
2. ☒ The allowed claim(s) is/are 1-20.
3. ☒ The drawings filed on 27 February 2004 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____


Jean Bruner Jeanglaude
Primary Examiner

Reasons For Allowance

Claims 1 – 20 are allowable.

1. The following is an examiner's statement of reasons for allowance: in combination with other limitations of the claims the prior arts made of record fail to suggest a digital to analog converter and method that comprise a first capacitance and a second capacitance configured in a first switching circuit wherein applying a complementary switching sequence corresponding to the first- pass switching sequence to the first switching circuit for converting the binary number results in a second voltage across the first capacitance and across the second capacitance; wherein, in applying the first-pass switching sequence, the first capacitance is charged to a conversion level a first number of times and the second capacitance is charged to the conversion level a second number of times; wherein in applying the complementary switching sequence, the first capacitance is charged to the conversion level the second number of times and the second capacitance is charged to the conversion level the first number of times; wherein, in applying the first-pass switching sequence, if the first capacitance is charged to the conversion level for a respective bit of the binary number then the second capacitance is not charged to the conversion level for the respective bit, and in applying the complementary switching sequence the first capacitance is not charged to the conversion level for the respective bit, but the second capacitance is; wherein, in applying the first-pass switching sequence, if the second capacitance is charged to the conversion level for the respective bit, then the first capacitance is not charged to the conversion level for the respective bit, and in applying the complementary switching

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sequence the second capacitance is not charged to the conversion level for the respective bit, but the first capacitance is; wherein the first-pass switching sequence and the corresponding complementary switching sequence form a conversion sequence for the binary number, wherein for each bit of the binary number, charge is redistributed between the first capacitance and the second capacitance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
3. Tan (US patent Number 4,399,426) discloses an on board self-calibration of analog-to-digital and digital-to-analog converters.
4. Kapral (US Patent Number 4,451,820) discloses a charge redistribution integratable DAC.
5. Kapral (US Patent Number 4,523,179) discloses an integratable DAC.
6. Olmstead et al. (US Patent Number 4,968,989) discloses a switched capacitor filter for use with a DAC.
7. Kerth et al. (US Patent Number 5,376,936) discloses a one-bit switched capacitor DAC with continuous time linearity.

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8. Signore et al. (US Patent Number 5,440,305) discloses a method and apparatus for calibration of a monolithic voltage reference.
9. Smith (US Patent Number 5,821,892) discloses a DAC system.
10. Schneider (US Patent Number 5,889,485) discloses a charge summing DAC.
11. Opris et al. (US Patent Number 5,889,486) discloses a split capacitor array for digital-to-analog signal conversion.
12. Watson et al. (US Patent Number 6,154,162) discloses a dual stage switched capacitor DAC with scrambled MSB's.
13. Yamamura (US Patent Number 6,693,574) discloses a DAC and delta sigma DAC.
14. Chuang (US Patent Number 6,768,436) discloses a method and circuit resetting delta sigma modulator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jean Bruner Jeanglaude
Primary Examiner
October 14, 2004